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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/910,171	MOHAMMAD, SALEEM CHISTY	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 23 are presented for examination.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1 – 3, 5 – 6, 14 – 16, and 18 – 19 are rejected under the judicially created doctrine of double patenting over claims 1 – 9 of U. S. Patent No. 6,675,305 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

4. The limitations for claims 1 – 3, 5 – 6, of current application: detecting that operation on a register and counter block is needed; enabling/disabling a clock signal; and executing the operation through employment of clock are taught by claims 1 – 3 and 6, of U.S. Patent No. 6,675,305.

5. The limitations for claims 14 – 16, and 18 – 19 of current application: detecting that operation on a register and counter block is needed; enabling/disabling a clock signal; and executing the operation through employment of clock limitations are taught by claims 4, 7, 2, and 6, of U.S. Patent No. 6,675,305.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application, which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

6. Claims 4, 7, 8 – 10, 11 – 13, and 21 – 23, are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 9, of U.S. Patent No. 6,675,305 in view of Shafir et al. [hereinafter as Shafir], US Patent 5,742,603.

7. The limitations for claims 4, 7, 8 – 10, 11 – 13, and 21 – 23, of current application: detecting that operation [update or to be programmed] on a storage component [register and counter block] is needed; providing [enabling/disabling] a clock signal; and reading the storage component [status register] through employment of clock are taught by claims 2, 4, 6, and 7, of U.S. Patent No. 6,675,305. However, the preamble of the application refers to media access control [MAC], which is one of the applications [Ethernet network application] of the USB peripheral interface of U.S. Patent No. 6,675,305.

Shafir teaches a system and method for integrating repeater management function, media access control [MAC] function, and bridging support functions combined into a single device and control the repeater functions under direction of access port and monitor repeater function and provide status via access port and to control bridge support function with the use of RMON

counters [inherently teaches reading of RMON counter functions] and status and control registers [inherently teaches reading, setting and resetting functions of counters and registers] [col. 2, lines 31 – 51, col. 3, lines 16 – 67, col. 4, lines 19 – 38, col. 5, lines 19 – 52, fig. 2].

It would have been obvious to one of ordinary skill in art, having teaches of Yik and Shafir before him at the time the invention was made, to modify the Ethernet media access control [MAC] logic having a power saving technique disclosed by Yik to include a system and method for integrating repeater management, media access control [MAC], and bridging functions into a single device provide greater network efficiency [col. 2, lines 22 – 25, and lines 27 - 61].

8. The limitations for claims 4, 7 – 13, 14 – 16, and 21 – 23, of current application: detecting that operation on a register and counter block is needed; enabling/disabling a clock signal; and reading the operation through employment of clock limitations are taught by claims 4, 7, 2, and 6, of U.S. Patent No. 6,675,305 identical to the claimed limitations as of claims 1 – 9 of U.S. Patent No. 6,675,305.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1 – 2, 4 – 6, 8, 10, 14 – 15, 17 – 19, 21, and 23 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Yik et al. [hereinafter as Yik], US 2003/0226050A1.

12. As to claim 1, Yik discloses a system and method comprising:

a. detecting [an event] that an operation [process activities]on a register and counter block [register and counter block is inherent to RX/TX process logic circuitry] is needed [process activities on RX/TX is needed][para 0031, on page 4];

b. enabling [by gating the gated clock] a clock signal [RX/TX clock] to the register and counter block [process logic circuitry][para 0021 on page 3]; and

c. executing [performing] the operation [process activities] on the register and counter block [register and counter block is inherent to RX/TX process logic circuitry] through employment of the clock signal [RX/TX clock] [para 0014, 0015, 0018, and 0019 on page 1, and page 2, fig. 1 – 3].

13. As to claim 8, Yik discloses a system and method for reading a storage component [108, Buffer] in a media access control component [100, MAC controller] comprising the steps of:

a. detecting [detecting RX event] an update [write] to the storage component [RX FIFO][para 0031, on page 4];

b. providing [by gating the gated clock] a clock signal [RX clock] to the storage component [RX clock] in response to detection of the update [RX event][para 0021 on page 3]; and

c. reading [receive logic receiving packets and processing] the storage component [buffer] through employment of the clock signal [clocking data into RX Control Logic, 138] [para 0031, on page 4, fig. 3].

14. As to claim 14, Yik discloses a system comprising:

a. detection unit [inherent to the event detection] that detects that an operation [process activities] on a register and counter [register and counter block is inherent to RX/TX process logic circuitry] block is needed [process activities on RX/TX is needed][para 0031, on page 4];

b. a clock enable unit [logic for gating the gated clock] that enables [starts] a clock signal [RX/TX clock] to the register and counter block [process logic circuitry] in response to a detection [event detection] that the operation [processing] is needed [packet processing of received packets]; and

c. application logic [function block] that executes [performs] the operation [process] on the register and counter block through employment [enabling] of the clock signal [RX/TX clock][para 0014, 0015, 0018, and 0019 on page 1, para 0021 on page 3, para 0031, on page 4, fig. 1-3].

15. As to claim 21, Yik teaches a system for performing an operation on a storage component [FIFO] in a media access control component [100, MAC] comprising:

a. clock gating logic [it is inherent to gating of gated clock] that detects [RX/TX event] that an operation [processing activities] on the storage component [FIFO] is to be performed and enables a clock signal [RX/TX clock] to the storage component [FIFO] in

response to a detection that an operation is to be performed [packet processing of received packets]; and

b. application logic [function block] that performs the operation [process] on the storage component [FIFO] through employment [enabling] of the clock signal [RX/TX clock][para 0014, 0015, 0018, and 0019 on page 1, para 0021 on page 3, para 0031, on page 4, fig. 1-3].

16. As to claims 2, 10, 15, and 23, Yik discloses to disable [stop] the clock signal after the operation is performed [all activities done][step 241 in fig.2].

17. As to claims 4, and 17, Yick discloses that the register and counter block [RX/TX process control logic circuitry] is in a media access control component [100, MAC media access controller, fig. 1].

18. As to claims 5, and 18, Yick discloses a frame processor [102, FP] with media access controller [100], and PHY interface [104] with detecting and determining receive event therefore, he teaches to interrupt frame processor [FP] and detecting an interrupt signal to processor is inherent function of processor.

19. As to claims 6, and 19, Yick discloses enabling the clock signal by gating the gated clock therefore; he teaches to employ [to use] the interrupt signal as a gating signal [para 0021, on page 3].

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 3, 7, 9, 16, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yik et al. [hereinafter as Yik], US 2003/0226050A1 as applied to claims 1-6, 8, 10, 14 – 19, 21, and 23 above, and further in view of Shafir et al. [hereinafter as Shafir], US Patent 5,742,603.

22. As to claims 7, 9, 20 and 22 Yik teaches a system and method of power saving for MAC Ethernet control logic by detecting [an event] that an operation [process activities] on a register and counter block [register and counter block is inherent to RX/TX process logic circuitry] is needed [process activities on RX/TX is needed][para 0031, on page 4]; enabling [by gating the gated clock] a clock signal [RX/TX clock] to the register and counter block [process logic circuitry][para 0021 on page 3]; and executing [performing] the operation [process activities] on the register and counter block [register and counter block is inherent to RX/TX process logic circuitry] through employment of the clock signal [RX/TX clock] [para 0014, 0015, 0018, and 0019 on page 1, and page 2, fig. 1 – 3].

However, Yik does not teach reading of at least one of a remote monitoring [RMON] counter and a status register in the register and counter block [processing logic of MAC].

Shafir teaches a system and method for integrating repeater management function, media access control [MAC] function, and bridging support functions combined into a single device and control the repeater functions under direction of access port and monitor repeater function and provide status via access port and to control bridge support function with the use of RMON counters [inherently teaches reading of RMON counter functions] and status and control registers [inherently teaches reading, setting and resetting functions of counters and registers] [col. 2, lines 31 – 51, col. 3, lines 16 – 67, col. 4, lines 19 – 38, col. 5, lines 19 – 52, fig. 2].

It would have been obvious to one of ordinary skill in art, having teaches of Yik and Shafir before him at the time the invention was made, to modify the Ethernet media access control [MAC] logic having a power saving technique disclosed by Yik to include a system and method for integrating repeater management, media access control [MAC], and bridging functions into a single device provide greater network efficiency [col. 2, lines 22 – 25, and lines 27 - 61].

23. As to claims 3, and 16, Shafir discloses to write the status word into memory [col. 4, lines 11 – 18] therefore, he teaches to upgrade and programming functions too.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 703-305-3994. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Brown can be reached on 703-308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
July 19, 2004

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